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(54) Solar array

(57) Improved solar cell circuit layouts and cell structures (12) that protect solar arrays located on spacecraft disposed in geosynchronous earth orbit from electrostatic discharge. An insulating material (20), such as RTV adhesive, for example, is used as a barrier that disposed in intercell gaps (23) between solar cells (12). The use of the insulating material (20) modifies sparking in the gaps (23) caused by electrostatic discharge so that, while the spark still occurs, it has different non-destructive characteristics. The use of the insulating material (20) causes no damage to other solar cell materials, such as a Kapton insulating layer or substrate used to support the solar cells. Furthermore, unique solar cell wiring schemes are provided that limit the voltage between adjacent solar cells to 50 volts or less.

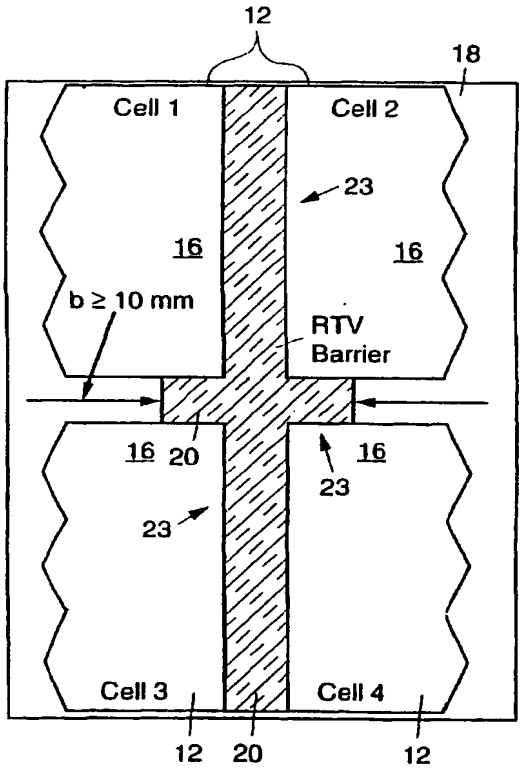

Fig. 11

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Description

[0001] The present invention relates generally to solar arrays, for example for use on spacecraft, and more particularly but not exclusively, to improved solar cell circuit layouts and solar cell structures for protecting solar arrays located on spacecraft disposed in geosynchronous earth orbit from electrostatic discharge.

[0002] During 1997, the assignee of the present invention launched five high-powered spacecraft which generate over 10 kW of electrical power at the beginning of their life. On two of those spacecraft there has been damage to the solar arrays during the first year of operation. Extensive analysis and ground testing has demonstrated that a damage mechanism exists in which electrostatic discharges occurring between pieces of cover glass and the solar cells on the solar arrays can be sustained by current from the solar array itself. Depending on the physical construction of the array, local heating can cause pyrolization of the insulation which separates the solar cells from the conductive substrate, thus resulting in short circuits of individual strings of solar cells. Susceptibility to this phenomenon is likely to increase throughout the industry as spacecraft power increases lead to larger solar arrays operating at higher voltages. However, analytical modeling and laboratory experimentation have verified the phenomenon and validated the preventative actions undertaken by the assignee of the present invention so that this phenomenon can be controlled on future spacecraft.

[0003] It would therefore be desireable to provide for technical approaches that protect solar cells on geosynchronously orbiting spacecraft from damage caused by electrostatic discharge. Accordingly, the present invention aims to provide improved solar cell circuit layouts and cell structures suitable for protecting solar arrays located on spacecraft disposed in geosynchronous earth orbit from electrostatic discharge.

[0004] According to the present invention, there is provided a solar array comprising:

a substrate;
a plurality of solar cells separated from each other by gaps;
an insulating barrier disposed between the substrate and the solar cells, and disposed in the gaps between solar cells, and for a predetermined distance in crossing gaps between series connected solar cells; and
cover glass disposed over the plurality of solar cells to cover exposed surfaces thereof.

[0005] The present invention provides for the use of an insulating material as a barrier, such as using RTV adhesive or insulating material, for example, disposed in intercell gaps between solar cells. The use of such insulating material modifies sparking in the gaps caused by electrostatic discharge so that, while the spark still occurs, it has different non-destructive characteristics. The use of the insulating material causes no damage to other solar cell materials, such as Kapton insulating material disposed between the solar cells and the substrate to support the cells. Furthermore, unique solar cell wiring schemes are provided that limit the voltage between adjacent cells to 50 volts or less.

[0006] In developing the present invention, a model was developed for spacecraft charging that shows that the solar panels of large geosynchronous earth orbit communications satellites can exhibit an "inverse potential gradient" in which the solar cell cover glass charges less negatively than the spacecraft body. The amount of inverse potential gradient is strongly dependent on the bulk resistivity of the cover glass.

[0007] A model of the arc discharge that can result from this potential gradient was also developed that shows that a plasma created by the discharge can trigger a sustaining arc, with current fed from the array itself. It has been found that there is a threshold cell-to-cell differential voltage below which the sustaining arc cannot be created, which may be why it has not been a problem with spacecraft in the past.

[0008] The arc discharge model has been verified by testing at NASA Lewis Research Center. This verification has shown that arrays that have been flown with high reliability for years (such as Intelsat VII, for example) can fail if they are operated at sufficiently high cell-to-cell voltage. Although heritage construction processes have been used, for both high power 100 V GaAs and Si arrays developed by the assignee of the present invention, the threshold for damage has been shown to be just at the limit of the normal operating range. The fact that the high power Si arrays currently in use have not been damaged can be attributed to detailed construction differences and it may be strongly influenced by the use of cover glass having a relatively low bulk resistivity.

[0009] In implementing the present invention, a number of construction techniques have been developed to provide a margin against failure from the secondary arc. Once the failure mechanism was understood, combining these techniques provides a very large margin to prevent the arc discharge phenomenon from occurring in the future. The corrective action implemented on future spacecraft to be launched by the assignee of the present invention will provide a safety margin significantly higher than that of previous solar arrays that have operated successfully for years.

[0010] Regarding the specifics in producing a solar array in accordance with a preferred embodiment of the present invention, the intercell voltage differential is lowered by 62.5 % by rewiring the solar panels, the voltage threshold at which damage can occur is increased by a factor of 3 to 4 by adding the insulating material barrier between cells, and the current available to the arc is decreased by a factor of 2 to 3 by adding solar cell string isolation diodes.

[0011] The susceptibility of solar arrays to electrostatic damage is a function of their construction details, which determines how susceptible they are to damage. However, using the principles of the present invention, solar arrays can safely be produced that operate at today's 10 kW power levels, and that will also operate at significantly higher power levels that will be used in the near future.

[0012] In order that the invention and its various other preferred features may be understood more easily, some embodiments thereof will now be described, by way of example only, with reference to the drawings in which:-

Fig. 1 illustrates a spacecraft anomaly that is corrected by the present invention;
Fig. 2 illustrates failure rate of a spacecraft as a function of time since launch;
Fig. 3 illustrates spacecraft charging as a function of cover glass resistivity;
Fig. 4 illustrates cover glass differential charging as a function of cover glass resistivity;
Fig. 5 illustrates cover glass resistivity;
Fig. 6 illustrates cover glass charging potential as a function of distance from the spacecraft main body;
Fig. 7 illustrates solar cells charge in response to space environment;
Fig. 8 illustrates that spacecraft charging causes a small arc to occur in the gap between solar cells;
Fig. 9 illustrates the spacecraft charging arc triggers a sustained discharge driven by the array string current and voltage;
Fig. 10 illustrates a top view of the array showing an intercell gap;
Fig. 11 illustrates the use of an insulating barrier between cells in accordance with the principles of the present invention;
Fig. 12 illustrates a test setup used to test the present invention;
Fig. 13 illustrates an example of solar array augmented discharge leading to failure;
Fig. 14 illustrates a measured GaAs coupon failure threshold;
Fig. 15 illustrates a measured Si coupon failure threshold;
Fig. 16 illustrates a GaAs coupon failure threshold with the present insulating barrier installed;
Fig. 17 illustrates a Si coupon failure threshold with the present insulating barrier installed;
Fig. 18 illustrates a solar cell layout in accordance with the present invention wherein the cell-to-cell voltage is limited to 50 V or less;
Fig. 19 illustrates that the insulating barrier protects exposed Kapton insulator;
Fig. 20 illustrates that each solar cell string is isolated by diodes, limiting the current available to an arc;
Fig. 21 illustrates a exemplary solar cell circuit layout in accordance with the present invention that is resistant to electrostatic discharge; and
Fig. 22 illustrates an exemplary solar cell circuit layout in accordance with the present invention that provides for electrostatic discharge current limiting.

[0013] Referring to the drawing figures, and in particular Fig. 1, anomalies observed on spacecraft 10 deployed by the assignee of the present invention are consistent with failures of strings 11 of solar cells 12 on solar arrays 13 (solar panels 13). The symptoms of the failures are low impedance shorts between solar cells 12 at different points within a string 11, and shorts between high voltage solar cells 12 and the array ground. All of the anomalies occurred when other instrumented satellites measured a charging environment characteristic of a solar substorm.

[0014] In a paper by Katz, et al. entitled "Mechanism for Spacecraft Charging Initiated Destruction of Solar Arrays in GEO," *36th AIAA Aerospace Sciences Meeting and Exhibit,* 1998, a theory and supporting laboratory data were presented, showing how small, low energy, spacecraft charging arcs on solar arrays can lead to larger, sustained discharges, in turn leading to permanent damage of the solar arrays 13. Since the Katz, et al. publication, additional work performed by the assignee of the present invention has led to an understanding of the phenomenon, of the existence of a cell-to-cell voltage threshold below which the sustaining arc cannot occur, and of the appropriate preventative action. Each step of this theoretical understanding has been empirically verified.

[0015] Two of the spacecraft 10 developed by the assignee of the present invention use Gallium Arsenide (GaAs) solar cells 12. These are the two spacecraft 10 that have suffered damage, with 18 out of 80 circuits (22%) having been damaged. Fig. 2 shows the cumulative failure history as a function of time since the launch of the spacecraft 10. As can be seen, the failure rate has decreased significantly with time.

[0016] The remaining three arrays 13 use Silicon (Si) solar cells 12. One of the 120 circuits on these spacecraft 10 has suffered an anomaly. Its signature is different from the others described herein, and it is not possible to tell from data available on the ground whether or not it is from the same cause. As will be shown, the likelihood of damage is a function of many of the detailed construction parameters of the array 13. Although the arrays 13 discussed herein are GaAs and Si, one should not conclude that GaAs, *per se,* is any more susceptible to damage than Si.

[0017] Spacecraft charging analysis using the NASA Charging Analyzer Program (NASCAP) is discussed in a paper by Katz, et al. entitled "The Capabilities of the NASA Charging Analyzer Program," *Spacecraft Charging Technology-1978,* NASA CP-2071, AFGL-TR-79-0082, edited by R. C. Fincke and C. P. Pike, p. 101,

1979. This paper identified the solar arrays 13 as the probable site of spacecraft charging initiated arcs.

[0018] For decades it has been known that 30-50 keV electrons in the magnetosphere can cause electrostatic potentials of several thousand volts to develop between different surfaces on the same spacecraft 10. Flight observations have shown that the large potential differences can lead to arc discharges. This phenomenon is discussed in papers by DeForest, entitled "Spacecraft Charging at Synchronous Orbit", *J. Geophys. Res., 77,* p 651, 1972, Mullen et al., entitled "Scatha Survey of High-Level Spacecraft Charging in Sunlight", J. *Geophys. Res., 91,* p. 1474, 1986, and Koons, entitled "Summary of Environmentally Induced Electrical Discharges on the P78-2 (SCATHA) Satellite", *J. Spacecraft and Rockets, 22,* p 425, 1983. Modern geosynchronous communications satellites are typically covered with conducting surfaces to prevent surface potential differences and arcing. The only nonconducting surfaces are usually pieces of solar cell cover glass 16 (shown in Figs. 7-11 and most clearly in Fig. 19).

[0019] The NASCAP program was used to analyze the electrical charging expected on the spacecraft 10, and to locate possible discharge sites. Because the actual environment is unknown, the calculations were performed using the NASA recommended "worst case" charging environment discussed in a paper by Purvis et al entitled *"Design Guidelines for Assessing and Controlling Spacecraft Charging",* NASA TP 2361, 1984. Parameters of the "worst case" charging environment are n_e = 1.12 x 10^6 m^{-3}, T_e = 12 keV, n_i = 2.36 x 10^5 m^{-3}, and T_i = 29.5 keV.

[0020] The analysis shows that a spacecraft 10 charges during substorms, even when it is in sunlight. The reason is that photoemission from the relatively small conducting area that is sunlit is exceeded by the charging currents to the large conducting areas that is in the dark if the front surface of the solar arrays 13 is steered towards the sun. In the presence of a charging environment, the chassis of the spacecraft 10 charges negative at an initial rate of about -5 V/s, as is shown in Fig. 3.

[0021] The front surface of the solar array 13, however, always faces the sun, and charge from the cover glass 16 is constantly bled off via photoemission (except during an eclipse, when the arrays 13 do not produce power). This leads to an inverted potential gradient in which the pieces of the cover glass 16 are less negatively charged than the underlying cell material and metallic interconnects. As is shown in Fig. 4, the potential difference between the cover glass 16 and the underlying cell increases at an initial rate of about 3 V/s. The photoemission current maintains the cover glass 16 near ambient potential.

[0022] Initially, the resistivity of the cover glass 16 was modeled as being effectively infinite. Further examination, revealed however, that if the bulk resistivity, *ρ,* of the cover glass 16 was less than about 10^{-3} Ω-m, then the maximum charge might be held below the threshold of electrostatic discharges. For example, for a cover glass 16 having a resistivity of 10^{13} Ω-m, the maximum voltage is limited as follows:

$$V = (\rho \, x \, t) \, I$$
$$= 8 \text{ x } 10^{12} \text{ x } 125 \text{ x } 10^{-6})10^{-6}$$
$$= 1000V,$$

where ρ = weighted average of the resistivity (Ω-m) of the cover glass and adhesive, t = 100 microns of glass and 25 microns of adhesive, and I = 10^{-6}A/m^{-2}.

[0023] Fig. 5 shows the bulk resistivity for various materials used in cover glass 16. As can be seen, the resistivity of CMZ cover glass 16, which has been used on GaAs arrays 13 produced by the assignee of the present invention, is high enough that it does not significantly limit the charging voltage. The resistivity of 0213 cover glass 16, which is used on both Si arrays and GaAs arrays now under construction by the assignee of the present invention, is sufficiently low that it reduces the maximum charge potential. The exact value is a function of the charging environment, as well as the exact temperature of the solar array 13 at the time. This is one possible explanation for the fact that the Si arrays 13 have not experienced troubles on orbit. For future spacecraft 10, by the assignee of the present invention is investigating switching to CMX or other lower resistivity cover glass 16 as standard practice.

[0024] The final step of the charging analysis is the recognition that the electrostatic potential is not constant along the array 13, increasing as the distance from the main body of the spacecraft 10 increases. Fig. 6 illustrates this, for a snapshot two minutes after a charging event is initiated, assuming infinite cover glass resistivity.

[0025] As can be seen in Fig. 6, the voltage on the fourth panel 13 is over 300 V, decreasing to 140 V on the first panel 13. Of the 18 failures on orbit, 7 have occurred on the fourth panel 13, or outermost panel 13, 4 on the third panel 13, and 2 on the first panel 13. The location of the remaining 5 failures is not known precisely, but it is known that they are not on the first panel 13. The inference is clear, in that, discharges occur first on the outermost panel 13. Once a discharge occurs, the spacecraft 10 is neutralized and the charging is reinitialized. If discharging continues to occur preferentially on the outermost panel 13, this will protect the inboard panels 13. The fact that failures occurred very early in life on the outermost panels 13 and have decreased significantly in frequency suggests that the remaining portion of the solar arrays 13 may continue to operate normally for the rest of the lifetime of the spacecraft 10.

[0026] The arcs described above have insufficient energy or currents to lead to permanent failures in the power system of the spacecraft 10. Further analysis sug-

gested that the short duration spacecraft charging arcs could trigger long duration discharges between solar cells 12; these discharges supported by the solar array current itself. The long duration discharges dissipate substantial energy, and can cause permanent damage to Kapton insulating material 19 (Fig. 19) on which the solar cells 12 are mounted. The effect on the Kapton material 19 is to turn this high resistance polymer into a low resistance carbonized ash. This process, pyrolysis, was previously reported in a paper by Stueber et al., entitled "Evaluation of Kapton Pyrolysis, Arc Tracking, and Flashover on SiOx-Coated Polyimide, Insulated Samples of Flat Flexible Current Carriers for SSF", NASA-CR 191106, 1993. The net effect is to short out the string 11 of solar cells 12, either between high and low voltage cells 12, or between cells 12 at different positions in the string 11 and the underlying substrate 18 which is at spacecraft chassis ground potential, as shown in Fig. 1.

[0027] A simple theoretical model was developed for generating a plasma by a discharge between the solar cell 12 and its cover glass 16. Figs. 7-9 sequentially illustrates what happens. First, the solar array 13 charges due to the space environment (Fig. 7). The insulated cover glass 16 is discharged due to photoemission of electrons, leading to a differential charge between the cover glass 16 and the solar cells 12. Next, an electrostatic discharge occurs between the cover glass 16 and a solar cell 12 (Fig. 8). This "triggering arc" 17 is known to occur at a differential voltage of several hundred volts. The discharge contains very little energy and is, of itself, harmless.

[0028] However, a plasma created by the triggering arc 17 can collect current from the array 13 itself, leading to a "sustained arc" 17a (Fig. 9). The energy in this discharge, the product of the discharge current and the plasma voltage, can be substantial, and can be sufficient to pyrolize the Kapton insulating material 19. Thus phenomenon has been captured on film in NASA Lewis Research Center (LeRC) tests described below, and is quite spectacular.

[0029] The trigger current model is for spherical expansion of the plasma generated during solar cell discharge. The energy in the discharge, the product of the discharge current and the charging voltage, generates a plasma at the arc site by ionization. The plasma is assumed to expand spherically from the arc site at a velocity of 3×10^4 m/s, a typical value based upon other experimental studies. The electron and ion plasma densities are shown to vary as $1/r^2$, where r is the distance from the arc site.

[0030] The saturation current density collectible from the arc discharge plasma is estimated assuming that the electrons in the plasma have a Maxwellian velocity distribution with a temperature of 1.5 eV, which is typical for low discharge generated plasmas. The saturation current is the maximum current that can flow into the plasma from the solar array 13 if the potential of the collecting solar cell 12 is above the plasma potential. If the saturation current is greater than the maximum current in the solar array 13, it will limit the current.

[0031] The maximum current carried by the trigger arc 17 is found by integrating the plasma thermal electron current density over the exposed conduction surface area of adjacent cells 12, as shown in Fig. 10.

[0032] Maximum circuit current is found by integration over x, the distance along the cell:

$$I_{max} = h \int_{-g}^{\infty} \frac{j_e(1)}{g^2 + x^2} dx = \pi \frac{h j_e(1)}{g}$$

where h is the cell height, g is the intercell gap distance, and $j_e(1)$ is the current density at a distance of one meter from the arc site.

[0033] For the geometry of the solar arrays 13 in orbit that were developed by the assignee of the present invention, the saturation current was found to be 2.6 A, for an assumed discharge voltage of 500 V. Coincidentally, the maximum current available from the solar array 13 is almost identical (2.1 to 2.6 Amps per circuit for the GaAs arrays 13, and 2.3 to 3.4 Amps per circuit for the Si arrays 13).

[0034] Fig. 11 illustrates the use of a protective insulating barrier 20 (RTV adhesive 20) installed in gaps 23 between cells 12 in accordance with the principles of the present invention. Using the same modeling techniques, and the geometry of GaAs arrays 13 developed by the assignee of the present invention, the maximum current is reduced from 2.6 Amps to 0.15 Amps, which is a reduction factor of 17.

[0035] Presented below is a summary of the sustaining current model developed by the assignee of the present invention.

Step 1: The plasma expands spherically from a spot (arc site) of diameter ≈ 10 μm,

$$n_i = \frac{I_i}{e v_i 4\pi r^2}.$$

Step 2: The arc electron current flows through a hemisphere

$$j_e = \frac{I_e}{2\pi r^2}.$$

Step 3: The scattering is dominated by classical electron-ion collisions

$$\nu_{ei} = 3.9 \times 10^{-12} n_e \Lambda T_e^{-3/2}$$

$$\Lambda = 30 - \ln(n_e^{1/2} T_e^{-3/2}).$$

Step 4: The classical conductivity is given by

$$\sigma = \varepsilon_0 \omega_p / \nu_{ei}$$

Step 5: The voltage drop found by integrating over the radius

$$V(r) = \int_{r_1}^{r} \frac{I_e}{\sigma 2\pi r^2} dr.$$

[0036] The intercell voltage threshold effect will now be discussed. The voltage drop calculated in step 5 above is the potential drop in the plasma due to the ohmic resistance of the plasma to the discharge current. The voltage drop is in the range of 40 V, for reasonable assumptions of emission spot radius and ion current. The solar array 13 only collects electron current if the cell-to-cell bias voltage is greater than the resistive drop in the arc plasma. The current collected drops exponentially for bias voltages less than the local plasma potential.

[0037] Laboratory tests have been performed which validate this theory and which have led to a further understanding of the mechanisms that are involved. The tests successfully reproduced the failure symptoms observed in orbit, and provided great insight into the details of the controlling mechanisms.

[0038] A simple model for the generation of a plasma by trigger arc discharge of the cover glass 16 to the solar cell 12 has thus been developed. This analytical model is supported by the experimental data from testing performed at the NASA Lewis Research Center. In these tests, a solar panel coupon is installed in a thermal vacuum chamber with the potential between cells 12 adjustable externally.

[0039] The test setup, shown in Fig. 12, provides an inverted voltage gradient between the cover glass 16 and the solar cells 12 and their substrate 18. A bias supply 25 is used to set the substrate and cell ground return negative relative to chamber ground. A plasma source 26 is used to flood the cover glass 16 with a low energy (1-2 eV) low density plasma and thereby maintain the potential of the cover glass 16 near the chamber ground. A solar array simulator (SAS) 27 is used to simulate the voltage and current from the solar array 13 and provides for the differential cell voltages which are necessary to create the sustaining arc. The bias supply 25 charges a capacitor 28. The value of the capacitor 28 and the bias supply voltage determine the energy available to the arc discharge.

[0040] This arrangement is actually more representative of a low earth orbit environment, and is thought to represent a significantly worst case scenario for geosynchronous earth orbit. Failures that occur infrequently in geosynchronous earth orbit can be systematically induced, leading to rapid verification of protective measures. The geosynchronous earth orbit environment has also been simulated in a solar thermal bacuum chamber of the present assignee. However, arcing at voltages below several thousand volts have not been induced. It appears that the phenomenon does not occur in a perfect vacuum, and a plasma medium must be present to initiate the arc.

[0041] The amount of energy that can be stored during spacecraft charging is proportional to the capacitance of the solar cell 12 and cover glass 16 combination. A capacitor 28 in the test setup shown in Fig. 12 is used to control the energy of the trigger arc. Capacitance values up to twice the capacitance of an entire solar panel 13 are used to demonstrate margin.

[0042] The number of arcs for a 30 minute period are plotted versus bias supply voltage. From these tests the arc threshold voltage between cover glass 16 and solar cell 12 is determined. The test also measures the current waveforms for all arc discharges. The instrumentation allows the initial trigger arc to be visible and the absence or presence of a sustaining arc can be observed. The SAS voltage is increased in steps to determine the safe intercell voltage operating range.

[0043] Test results from the solar array 12 for a GaAs solar cell coupon with the same construction as on the on-orbit spacecraft 10 is shown in Fig. 13. More specifically, Fig. 13 illustrates solar array augmented discharge leading to failure. The solar cell bias was set to 80 V and the solar array current limit set to 2.25 Amps, close to the limit of the actual on-orbit operating conditions. The current supplied by the solar array 13 rises immediately to the current limit value. The dissipation of this large initial circuit current at the collecting cell 12 resulted in overheating and sustaining of the discharge beyond the 100 μsec of the trigger arc. The result was a cell-to-cell and cell-to-substrate short.

[0044] A number of tests similar to the one described above have been performed. The results show that failures can be induced in both the Si and the GaAs arrays 13 of the type launched by the assignee of the present invention. As predicted by the model, there is a voltage threshold value below which the trigger arc extinguishes itself within μsec, although the exact value of the threshold cannot be determined because it is dependent upon the precise geometry of the arc site.

[0045] Figs. 14 and 15 show that the onset of failure is just at the boundary of the on-orbit cell operating regime. No current to the solar cells 12 was observed in any NASA LeRC testing for cell voltages below 60 V, which is consistent with the magnitude of the threshold predicted by the model described above.

[0046] Testing of samples with the insulating (RTV) barrier 20 installed in the gap between cells 12, as

shown in Fig. 11, has demonstrated the effectiveness of the insulating (RTV) barrier 20, with the failure threshold being increased significantly beyond the operating regime. This is shown in Figs. 16 and 17. At the present time, both Si and GaAs coupons, manufactured in accordance with the principles of the present invention that will be used for future flights, are undergoing testing at NASA LeRC. The test procedure is set up to demonstrate margins of safety with respect to generation of a sustaining arc of at least a factor of 2 in voltage, and at least a factor of 2 in discharge energy (twice the capacitance equal to an entire panel 13). A minimum of 240 arcs are recorded for each case in the test matrix.

[0047] Testing of a GaAs coupon with insulating (RTV) barrier 20 installed has been completed. Discharge occurred at inverse gradient voltages of 290 to 530 V, and discharge voltage increases with time which could indicate that the threshold increases subsequent to arcs occurring at "weaker" locations.

[0048] The coupon experienced over 1000 arc discharges. The current recordings during the discharges showed that the insulating (RTV) barrier 20 is successful in limiting the flow of current into the plasma formed by the trigger arc. Current from the solar array simulator was generally in the 0.2 to 0.4 A range during the 50 to 100 μsec duration of the discharge. There were no cell-to-cell or cell-to-substrate shorts, and there were no instances of sustained arcing being fed by the solar array simulator. The conclusion is that the insulating (RTV) barrier 20 is effective in preventing the sustaining arc, as predicted by theory. In fact, previous experimental samples subjected to testing at far higher voltages showed that the ultimate damage occurred beyond the insulating (RTV) barrier 20 and that much higher cell-to-cell voltages were required to initiate such damage.

[0049] For future high power spacecraft to be launched by the assignee of the present invention, three corrective actions have been undertaken, any of which is sufficient to prevent damage from the phenomenon described in this paper. Together, significant margin is demonstrated.

[0050] First, solar array panels 13 are wired in accordance with the principles of the present invention so that the voltage between adjacent cells 12 is 50 V or less, as is shown in Fig. 18. The previous high powered spacecraft 10 had cases of 80 V (GaAs) and 75 V (Si) differentials between adjacent cells. Extensive analysis is used to ensure that this differential limit is not exceeded for various combinations of shunted and unshunted strings 11 of solar cells 12, shadowing cases, and cases of failed strings 11. The assignee of the present invention typically operates arrays at voltages up to 50 V, with excellent reliability results.

[0051] Second, as shown in Fig. 11 and in detail in Fig. 19, the insulating barrier 20, such RTV adhesive 20 or insulating material 20, is inserted in all gaps 23 between cells 12, and for a distance of at least 10 mm in the crossing gaps between series connected cells 12. As is shown in Fig. 19, the structure of the improved solar array 13 comprises a substrate 30 having an aluminum core 31 surrounded by a graphite skin 32. The Kapton insulating layer 19 is diposed on top of the substrate 30. The (RTV) insulating material 20 is disposed between the Kapton insulating layer 19 and bottom surfaces of the solar cells 12 and in the gaps 23 between the solar cells 12. Cover glass 16 covers exposed surfaces of the the solar cells 12. Testing of sample solar arrays 13 during the development of this process has shown that it increases the threshold for damage to about 200 V.

[0052] Third, an as is shown in Fig. 20, for arrays 13 in orbit, there are as many as five GaAs strings 11 in parallel, and as many as three Si strings 11 in parallel, to form a "circuit". Each circuit utilizes an individual solar array drive assembly (SADA) slip ring, and is connected to an individual switching shunt element (see Fig. 1). This arrangement provides up to 3.4 Amps (Si) and 2.6 Amps (GaAs) to feed the discharge.

[0053] Future GaAs arrays will use larger cells 12, such that the individual strings 11 will have current capability substantially identical to the Si arrays 13. Parallel strings 11 will be separated by diodes 22, as is shown in Fig. 20, on all unlaunched spacecraft 10 so that the most current available to an arc will be 1.1 A for both the Si and GaAs panels 13. This has the inherent benefit of a significant increase in calculated reliability, even without considering the phenomenon described in this paper, at a small penalty in efficiency of the solar array 13.

[0054] Additional details regarding the structures discussed with reference to Figs. 18-20 are presented below. In particular, two high voltage solar array designs are shown in Figs. 21 and 22, respectively. The present invention provides for techniques for designing solar panels 13 for use at high power levels. As was mentioned previously, prior solar panel designs that are to operated at voltages greater than 70 V, for example, had the potential to fail when the space environment caused electrostatic discharge. The present invention allows use of solar panel voltages over 70 volts. Solar panels 13 produced in accordance with the principles of the present invention are more robust to electrostatic discharge.

[0055] A first exemplary circuit layout accordance with the present invention is shown in Fig. 21 that is resistant to electrostatic discharge. Solar cell circuits to be used for spacecraft power systems may be assembled from all commonly used photovoltaic devices, including silicon, gallium arsenide and multi-bandgap cells. As is shown in Fig. 21, the solar cells 12 are arranged on the solar panels 13 in a pattern that prevents adjacent solar cells 12 from having voltage potential greater than 50 volts. A spiral interconnection arrangement is used to serially interconnect the solar cells 12 together. Furthermore, isolation or blocking diodes 22 are used to limit reverse current through a shorted circuit.

[0056] Referring to Fig. 22, it illustrates a exemplary

solar cell circuit layout in accordance with the present invention that provides for electrostatic discharge current limiting. When circuits are to be connected in parallel, the prevention of reverse current through a shorted circuit should be limited to less than 1.5 Amps. The use of the isolation or blocking diodes 22 is one means for limiting the reverse current through the shorted circuit. The circuit layout shown in Fig. 22 provides for electrostatic discharge current limiting. The addition of insulating material (the insulating barrier 20) disposed between the solar cells 12, such as RTV insulating material 20 or adhesive 20, for example, as is illustrated in Fig. 19, provides further protection from electrostatic discharge for voltages in excess of 100 volts.

[0057] Thus, improved solar cell circuit layouts including means for protecting solar arrays located on spacecraft disposed in geosynchronous earth orbit from electrostatic discharge have been disclosed. It is to be understood that the above-described embodiments are merely illustrative of some of the many specific embodiments that represent applications of the principles of the present invention. Clearly, numerous and other arrangements can be readily devised by those skilled in the art without departing from the scope of the invention.

Claims

1. A solar array (13) comprising:

   a substrate (31);
   a plurality of solar cells (12) separated from each other by gaps (23);
   an insulating barrier (20) disposed between the substrate and the solar cells (12), and disposed in the gaps (23) between solar cells (12), and for a predetermined distance (b) in crossing gaps between series connected solar cells (12); and
   cover glass disposed over the plurality of solar cells to cover exposed surfaces thereof.

2. The solar array of Claim 1 further comprising an insulating layer (19) disposed between the substrate (31) and the plurality of solar cells (12).

3. The solar array of Claim 1, further comprising an insulating layer (19) disposed on the substrate (31), the insulating barrier layer (20) being disposed between the insulating layer (19) and the solar cells (12).

4. The solar array of Claim 2 or 3 wherein the insulating layer (19) comprises Kapton material.

5. The solar array of any preceding claim wherein the substrate (31) comprises an aluminum core 31 surrounded by a graphite skin (32).

6. The solar array of any preceding claim wherein the insulating barrier (20) comprises an insulating adhesive.

7. The solar array of Claim 6 wherein the insulating adhesive comprises RTV adhesive.

8. The solar array of any preceding claim wherein the predetermined distance (b) is at least 10 mm in the crossing gaps between series cells.

9. The solar array of any preceding claim wherein the solar cells (12) are wired together so that the voltage between adjacent cells is 50 V or less.

10. The solar array of Claim 9 wherein the solar cells (12) are wired together in a spiral interconnection pattern to serially interconnect the solar cells together, and which prevents adjacent solar cells from having voltage potential greater than 50 volts.

11. The solar array of any preceding claim further comprising a plurality of isolation diodes (22) coupled to respective outputs of interconnected ones of the solar cells (12) to limit reverse current through a shorted solar cell.

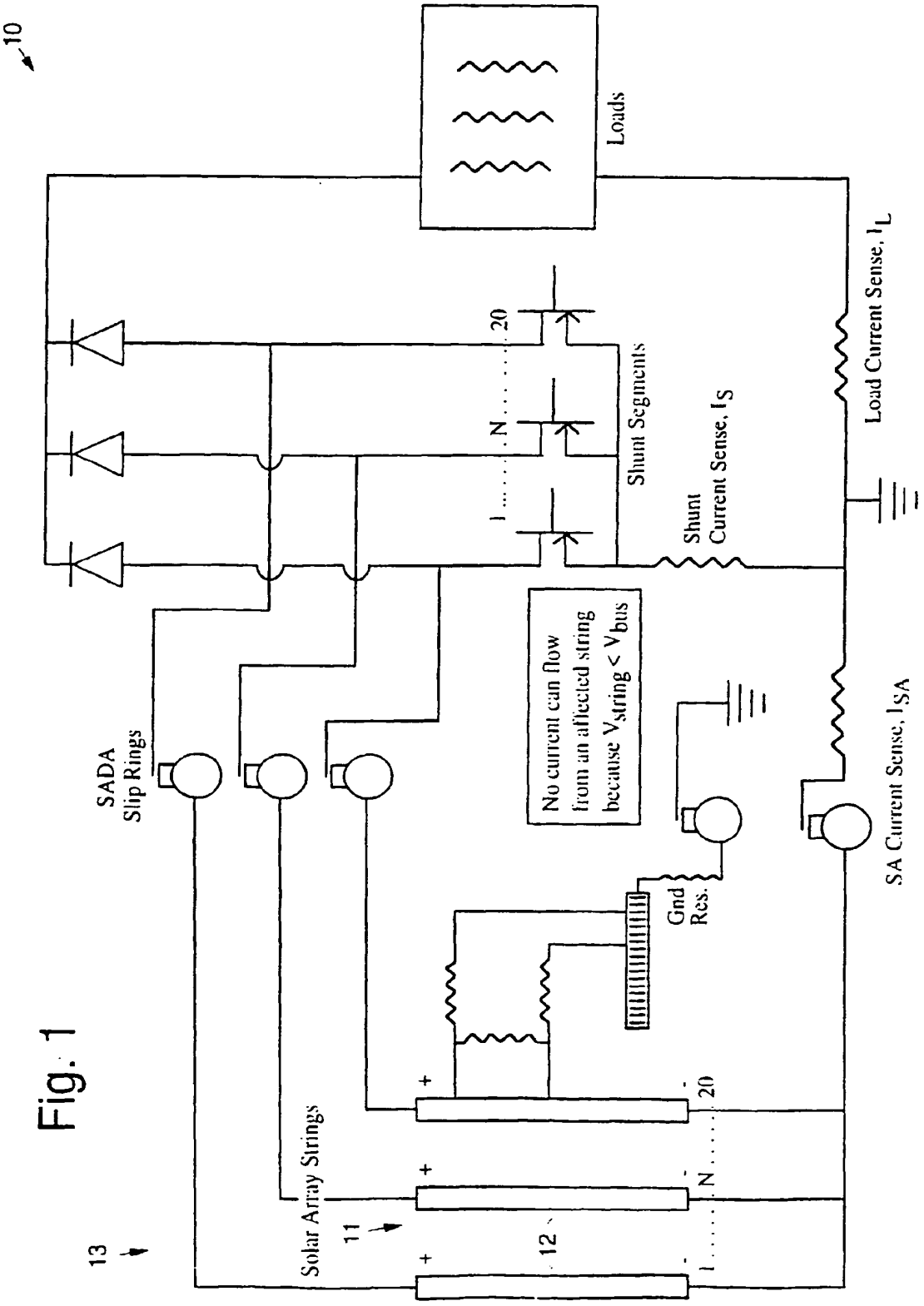


Fig. 1

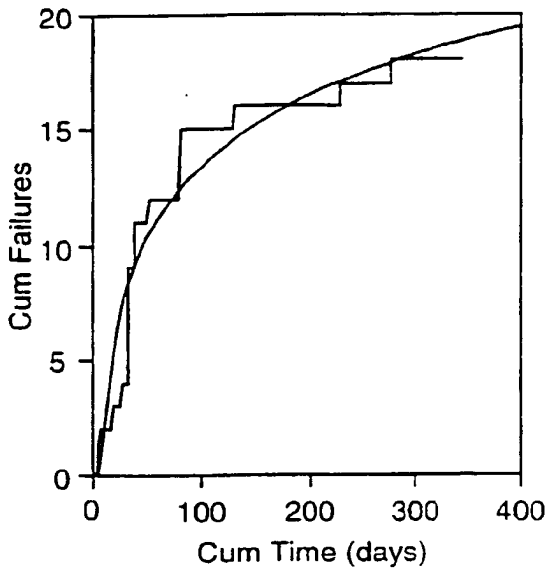


Fig. 2

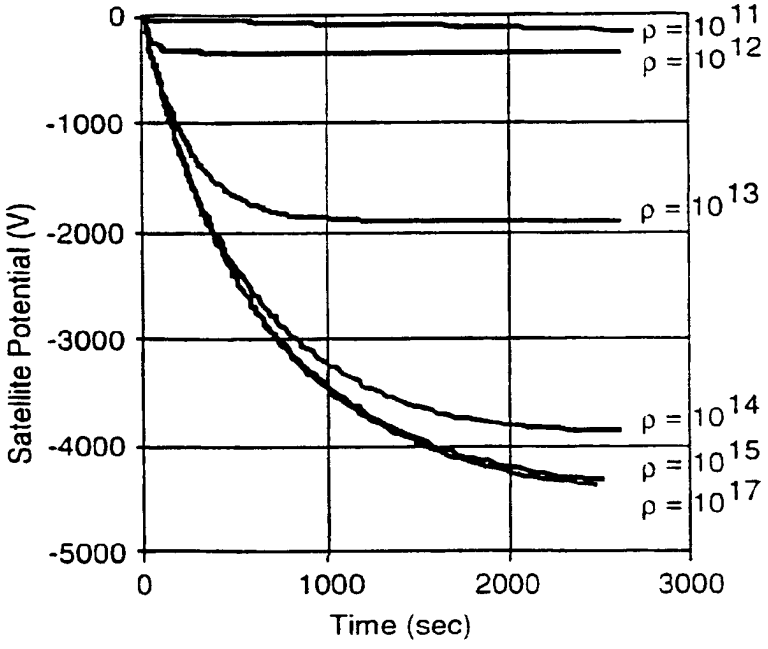


Fig. 3

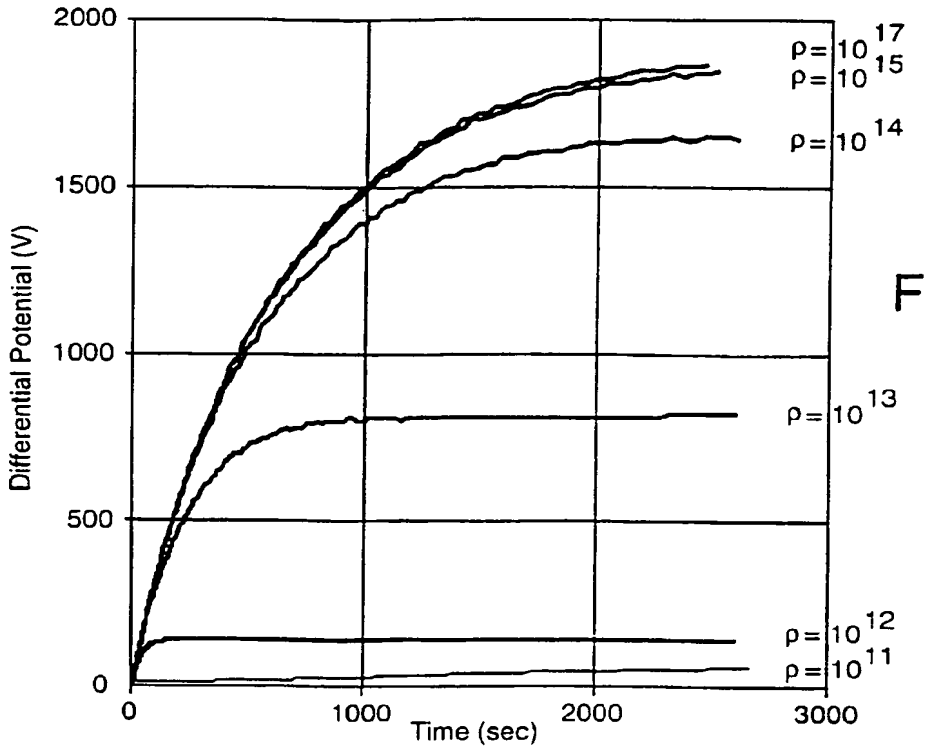


Fig. 4

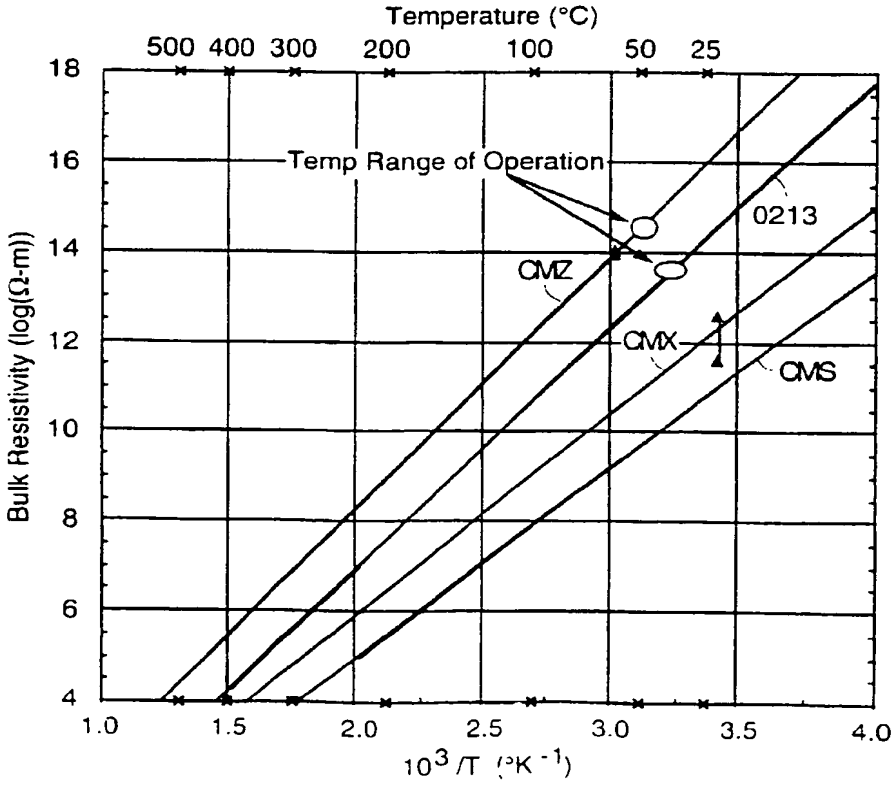


Fig. 5

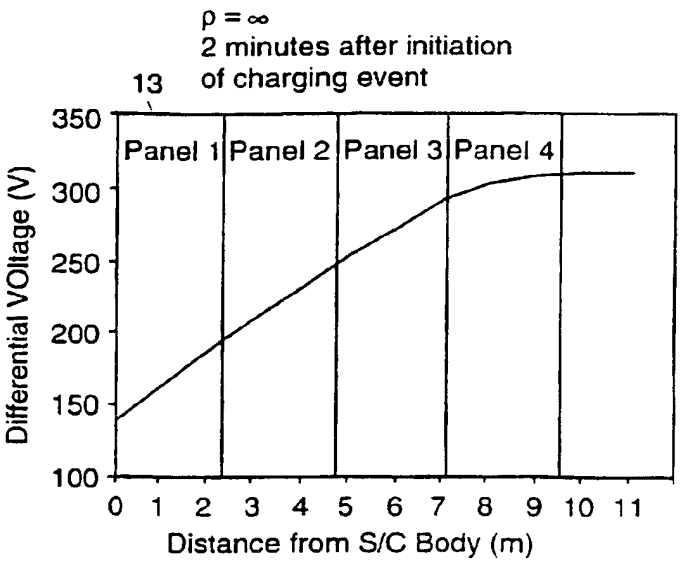
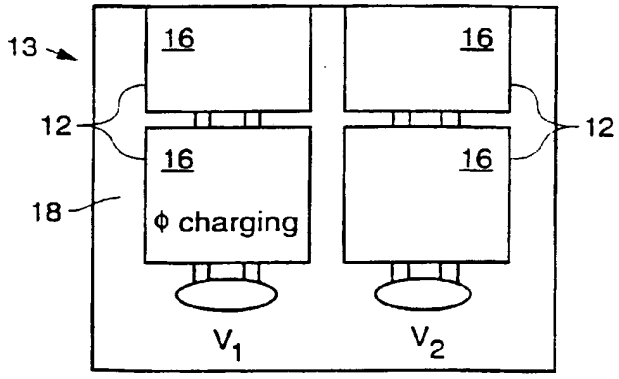


Fig. 6



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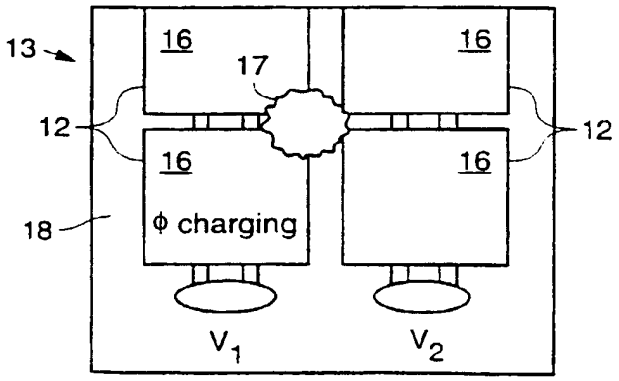


Fig. 8

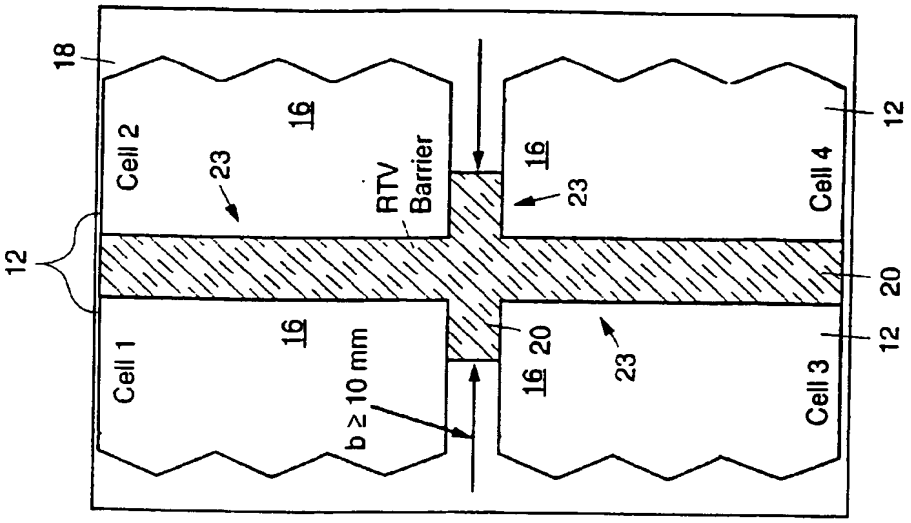


Fig. 11

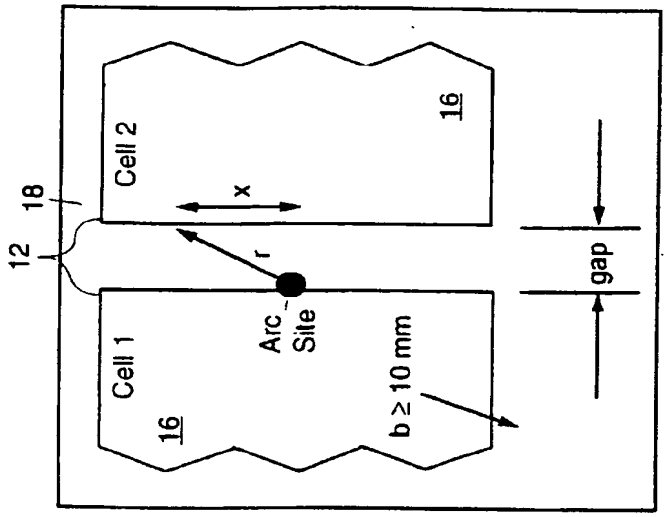


Fig. 10

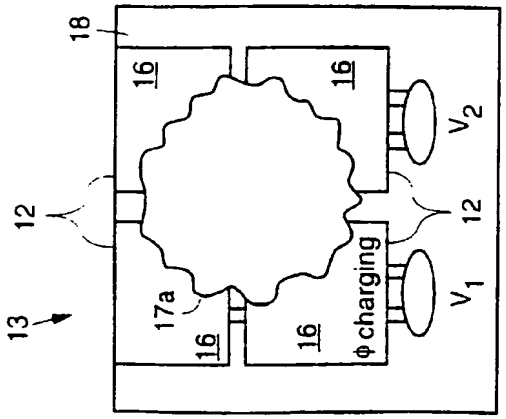
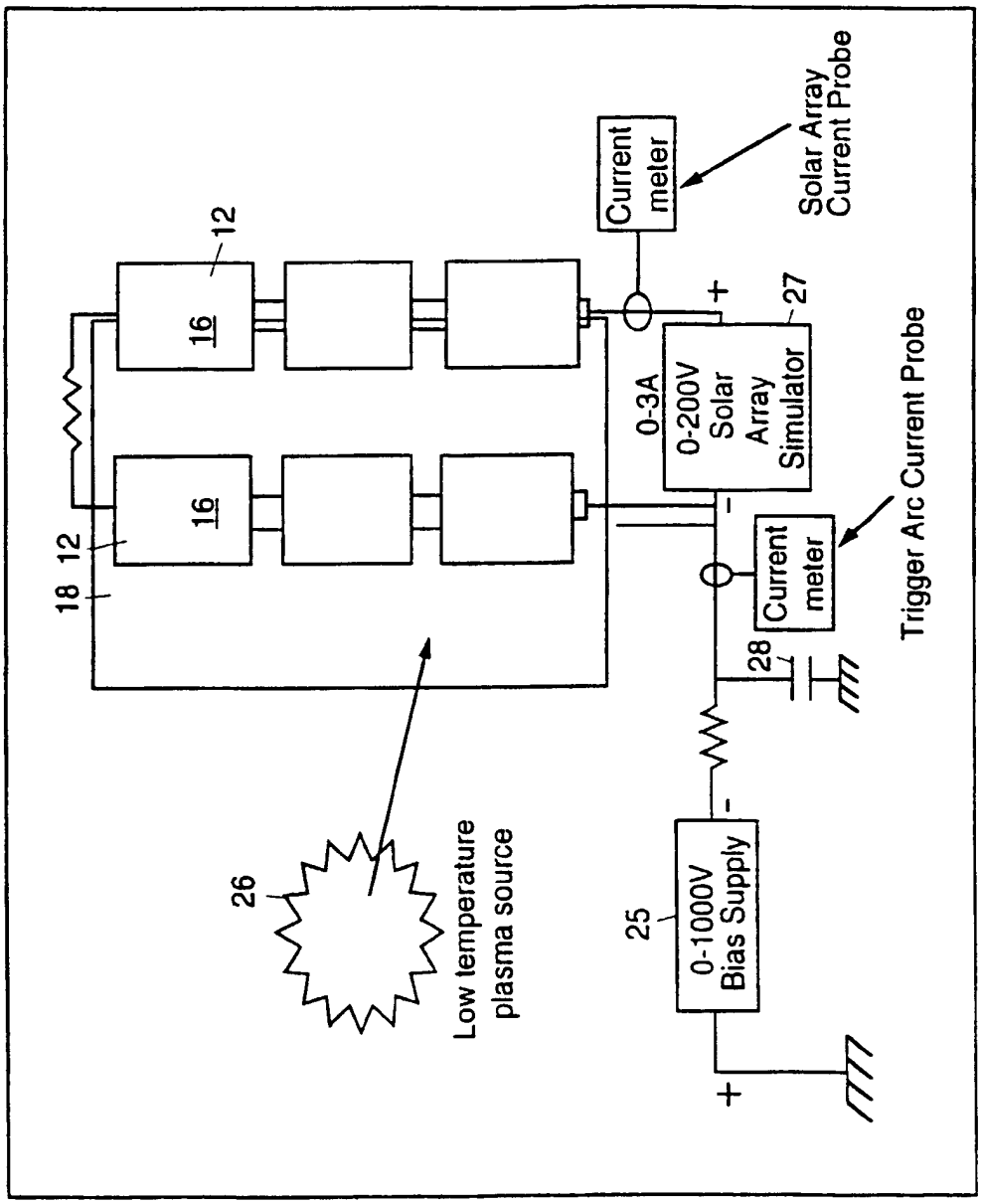


Fig. 9

Fig. 12



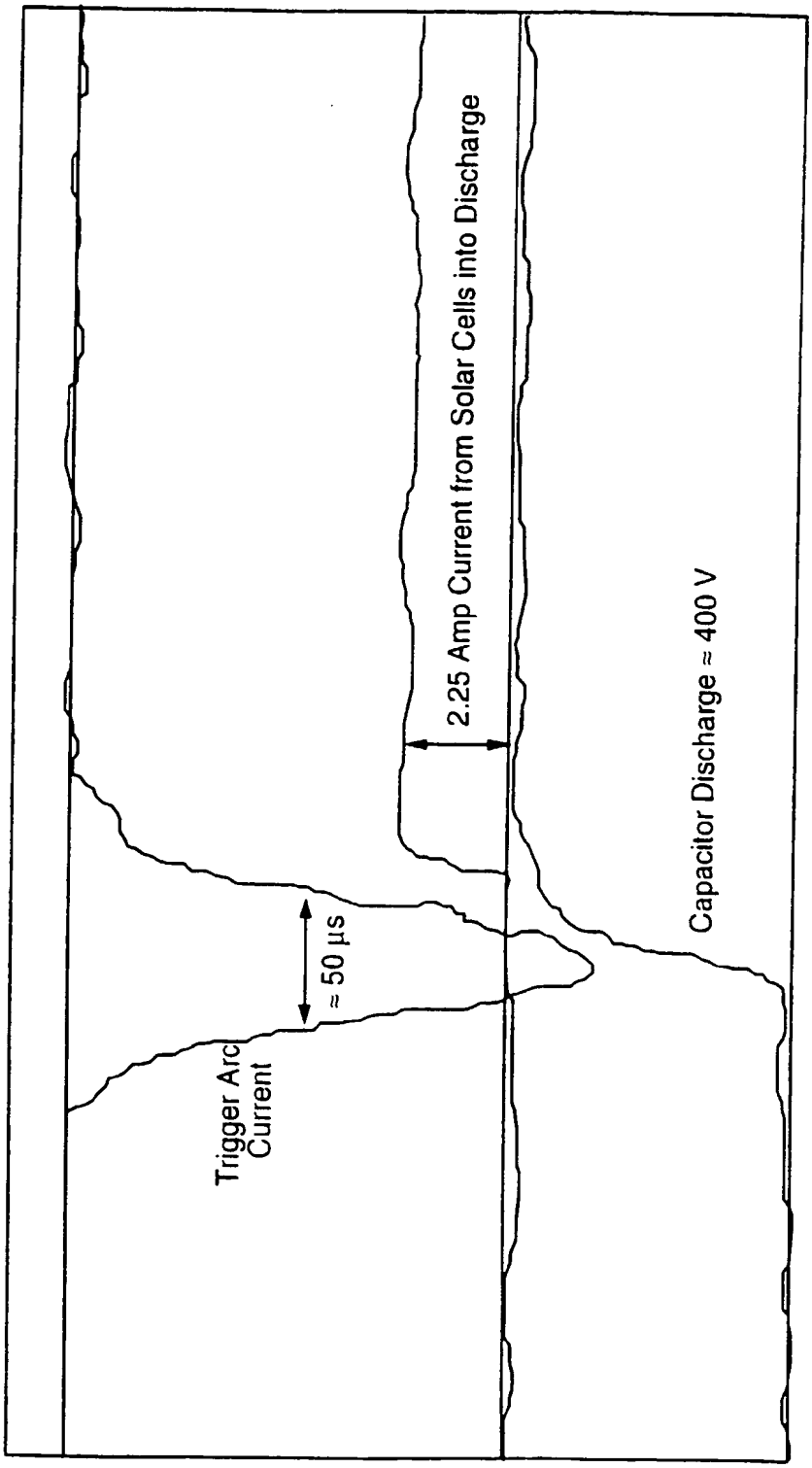


Fig. 13

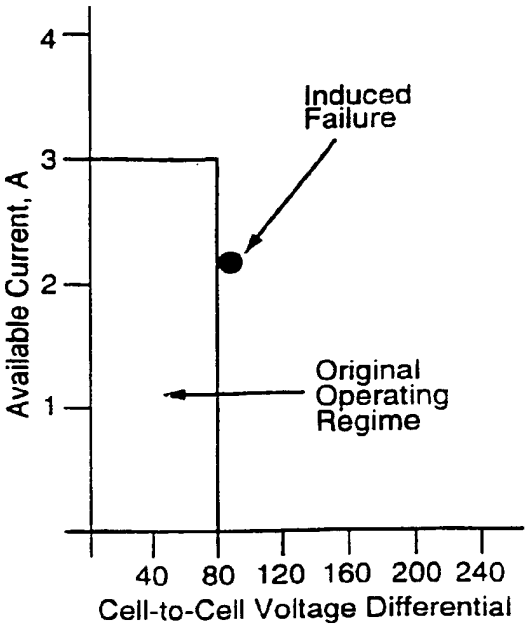


Fig. 14

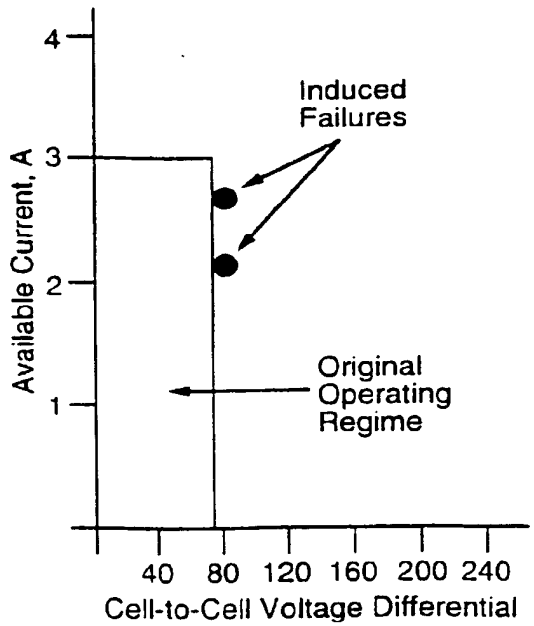


Fig. 15

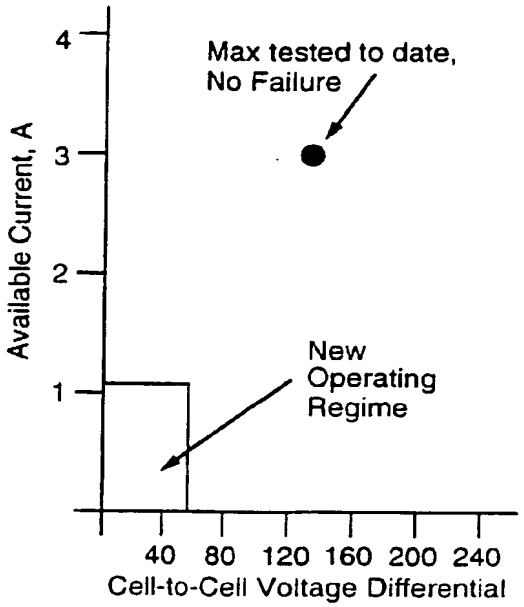


Fig. 16

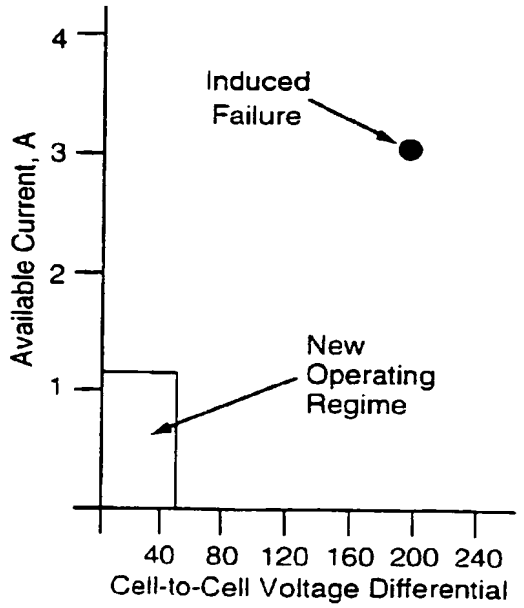


Fig. 17

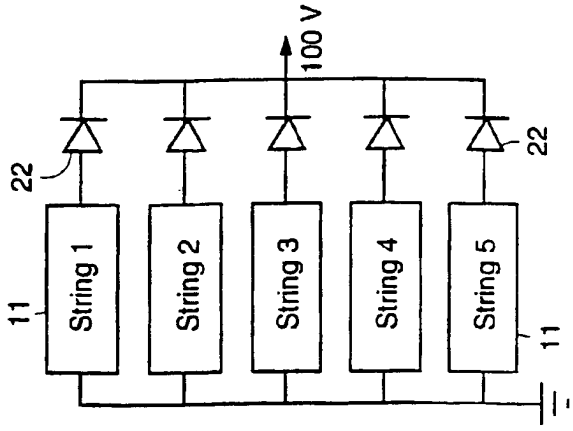


Fig. 20

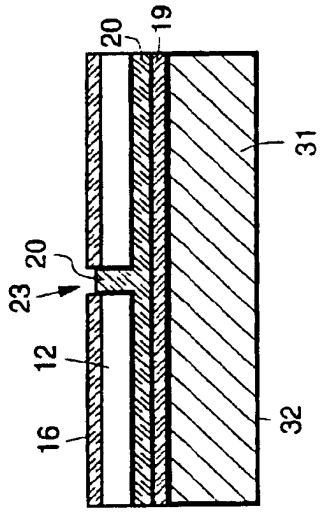


Fig. 19

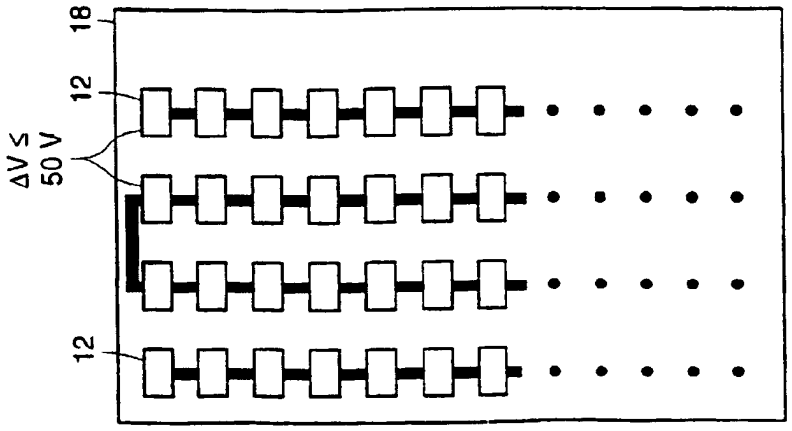


Fig. 18

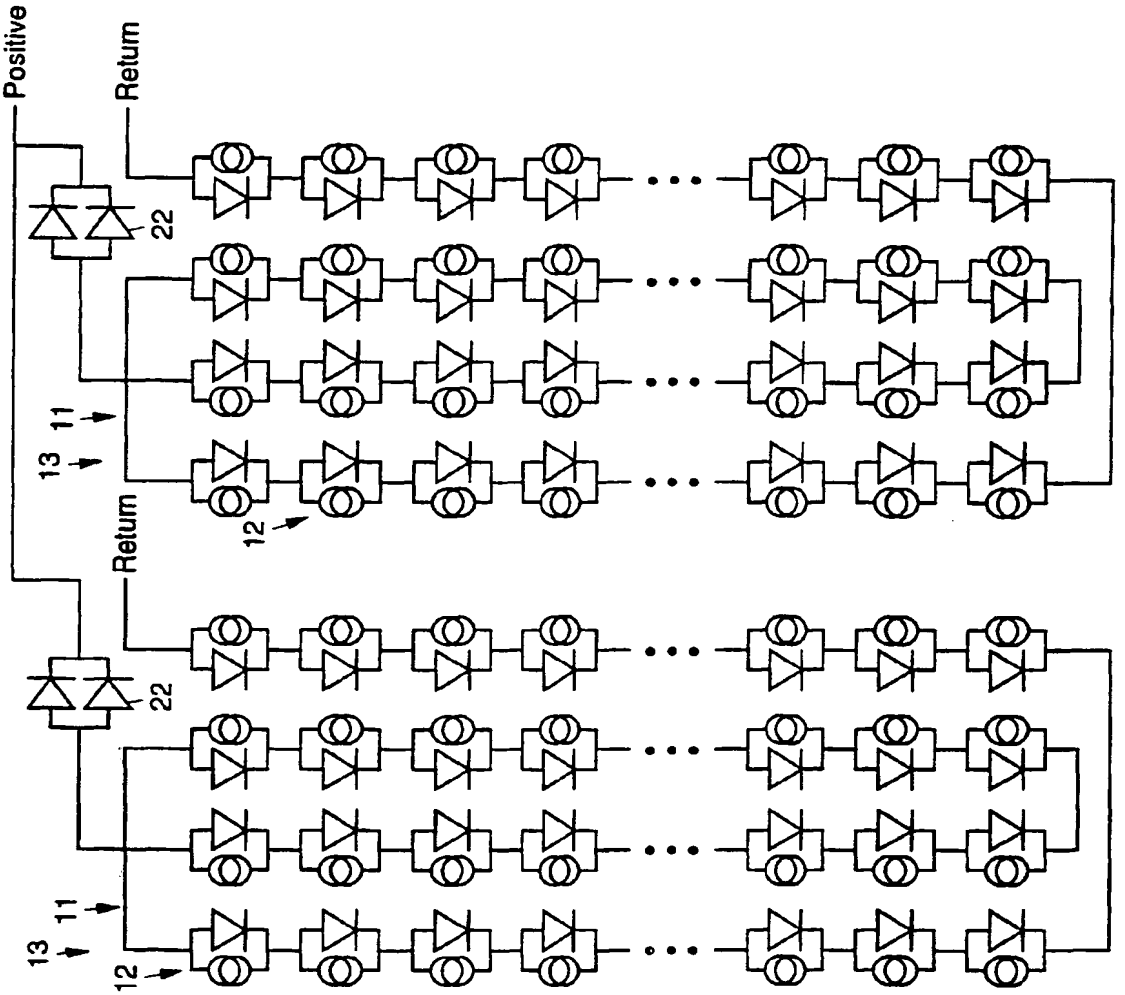


Fig. 22

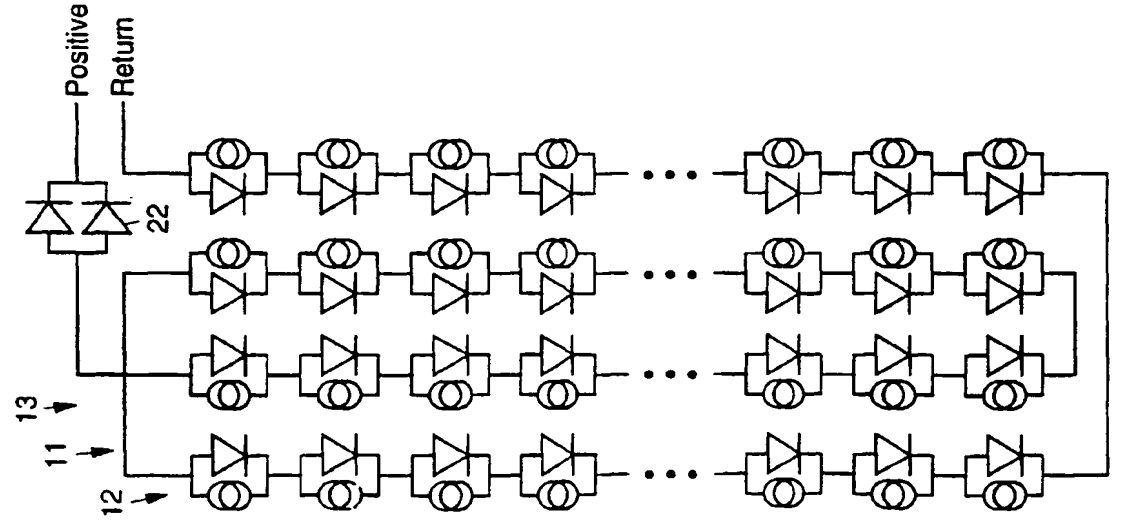


Fig. 21

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(11) EP 0 938 141 A3

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(54) Solar array

(57) Improved solar cell circuit layouts and cell structures (12) that protect solar arrays located on spacecraft disposed in geosynchronous earth orbit from electrostatic discharge. An insulating material (20), such as RTV adhesive, for example, is used as a barrier that is disposed in intercell gaps (23) between solar cells (12). The use of the insulating material (20) modifies sparking in the gaps (23) caused by electrostatic discharge so that, while the spark still occurs, it has different non-destructive characteristics. The use of the insulating material (20) causes no damage to other solar cell materials, such as a Kapton insulating layer or substrate used to support the solar cells. Furthermore, unique solar cell wiring schemes are provided that limit the voltage between adjacent solar cells to 50 volts or less.

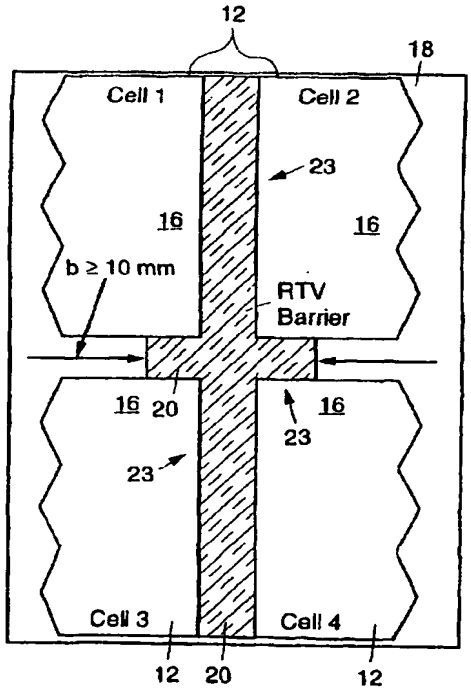

Fig. 11

EP 0 938 141 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 1162

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	GB 2 224 391 A (GEN ELECTRIC) 2 May 1990 (1990-05-02) * page 5, line 26 - page 7, line 11; figures 3,4 *	1-3,6,7	H01L31/042 H01L31/048
X	PATENT ABSTRACTS OF JAPAN vol. 011, no. 152 (E-507), 16 May 1987 (1987-05-16) & JP 61 289675 A (SHARP CORP), 19 December 1986 (1986-12-19) * abstract *	1,6	
A	SANKARAN, M. ET AL.: "On the development of solar arrays for INSAT 2A and 2B" PROCEEDINGS OF THE EUROPEAN SPACE POWER CONFERENCE, vol. 2, 4 - 8 September 1995, pages 649-652, XP002116582 Poitiers, France * abstract; figure 3 *	1-7	
A	LA ROCHE, G.J. ET AL.: "Long term thermal cycling tests on gold interconnected solar cells" PROCEEDINGS OF THE EUROPEAN SPACE POWER CONFERENCE, vol. 2, 4 - 8 September 1995, pages 495-500, XP002116583 Poitiers, France * figures 1-3; table 1 *	1,3-8	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 September 1999	Acco, S

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X : particularly relevant if taken alone
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27-09-1999

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2224391 A	02-05-1990	FR 2638568 A	04-05-1990
		IT 1239117 B	28-09-1993
		JP 2177576 A	10-07-1990
		DE 3935826 A	13-06-1990
JP 61289675 A	19-12-1986	JP 1707415 C	27-10-1992
		JP 3060186 B	12-09-1991

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82